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Research and Development Technical Report
ECOM - 0039 - 7

MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

7TH QUARTERLY REPORT

By

Y. ANAND R. BILOTTA

APRIL 1978

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MM&T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH POWER BULK SEMICONDUCTOR LIMITERS

SEVENTH QUARTERLY REPORT

23 December 1977 to 22 March 1978

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Confirmatory Samples consisting of Twenty (20) X-band bulk limiters and multi-stage clean-up diode limiters were assembled. Bulk limiters were fabricated from high resistivity silicon with ρ = 8,000 - 15,000 ohm-cm, p-type, uncompensated ⟨111⟩ orientation from Wacker Chemical Company. These bulk limiters exhibit 3.0 dB bandwidth of 0.71 - 1.2 GHz and low insertion loss of 0.4 to 0.6 dB. New passivation schemes are being investigated in order to reduce the

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insertion loss of bulk limiters and also to improve the power handling capability of the bulk limiters.

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ABSTRACT

Confirmatory Samples consisting of twenty (20) X-band bulk limiters and multi-state clean-up diode limiters were assembled. Bulk limiters were fabricated from high resistivity silicon with ρ = 8,000 - 15,000 ohm-cm, p-type, uncompensated $\langle 111 \rangle$ orientation from Wacker Chemical Company. These bulk limiters exhibit 3.0 dB bandwidth of 0.71 - 1.2 GHz and low insertion loss of 0.4 - 0.6 dB. New passivation schemes are being investigated in order to reduce the insertion loss of bulk limiters and also to improve the power handling capability of the bulk limiters.

PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per U.S. Army Electronics Command Technical Requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time, (2) high power capability, (3) insertion loss, and (4) VSWR.

A total of fifteen (15) engineering sample limiters, twenty (20) confirmatory sample limiters and fifty (50) pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G, and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR No. 15, dated December 1976, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include iris formation, circuit configuration, material characterization and chip mounting. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phases II, III, and IV a single device design will be produced.

The major effort of this program will be realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually, any of the goals described can be currently obtained. Recognizably, it is the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

I. OBJECTIVE

The objective of the current Manufacturing Methods and Technology Engineering program is to establish the producibility of the X-band bulk semiconductor limiter and the X-band bulk semiconductor lower power diode multistage limiter by mass production techniques. Achieving the performance goals of the program represents a formidable engineering task. These goals, from SCS-486 are summarized below.

A. Function Description

The high power, solid state, limiter described herein will operate in the frequency band 9.0 - 9.65 GHz. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a common semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

B. Mechanical Characteristics

The bulk semiconductor limiter structure will have the following performance objectives:

Weight:	7.0 oz max
Input Flange:	mates with UG-40B/U choke flange
Output Flange:	mates with UG-135/U cover flange
Mounting Position:	any
Cooling:	conduction

C. Electrical Characteristics

The bulk semiconductor limiter will have the following objectives:

Peak RF input power:	30 kW, duty cycle = 0.001%
1 μsec pulses continuous:	10 kW, duty cycle = 0.01 %
Insertion loss:	0.7 dB (max)
Low level VSWR:	1.4:1 (max)
Recovery time:	0.8 μsec (max)
Flat leakage:	50 mW (max), for 30 kW, 0.001 duty cycle, 1 μsec pulse
Spike leakage:	750 mW (max), for 30 kW, 0.001 duty cycle, 1 μsec pulse
External bias:	none

D. Absolute Rating Objectives

PARAMETER	SYMBOL	MIN	MAX	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P		30	kW
Average Power	P_a		100	W
Ambient Temp	T_A	-55	+85	^oC
Altitude	--		50,000	ft

II. INTRODUCTION

This report covers the period from 23 December 1977 to 22 March 1978. During this period, the work was concentrated in the areas of semiconductor wafer processing, device fabrication and RF testing of bulk limiters.

Twenty (20) Confirmatory Samples were fabricated and tested for their RF performance. New passivation schemes are being investigated in order to reduce the insertion loss of bulk limiters and also to improve the power handling capability of the bulk limiters.

The subsequent sections of this report describes in greater detail the work performed and results achieved to date.

III. FABRICATION AND RF TESTING OF THE CONFIRMATORY SAMPLES

During this quarter, bulk limiters were fabricated for the twenty (20) piece Confirmatory Sample requirement. Bulk limiter chips from various runs were mounted in X-band gold plated copper irises and then bulk limiters were tuned to the proper center frequency. The bulk limiters were tested for bandwidth, recovery time, insertion loss, and power handling capability. These results are shown in Table I.

The clean-up limiters were then fabricated and pretuned for insertion loss, VSWR and isolation.

Subsequently, each bulk limiter was mated with a clean-up limiter and the entire package was finally tuned for insertion loss and VSWR. This low RF power performance data is given in Table II.

Final tuning of the package was accomplished solely by adjusting the position of the clean-up limiters and tuning screws. No tuning was performed on the bulk limiters after its center frequency had been set.

BULK LIMITER	f_o (MHz)	BW (MHz)	RECOVERY TIME (μs)	FLAT POWER (W)
16A-12	9300	1060	1.5	71
16A-2	9340	765	2.1	50
16A-47	9325	1010	2.3	90
17D-13	9320	840	1.2	50
16A-45	9350	1140	1.9	95
16A-1A	9325	910	1.8	55
17A-42	9350	970	1.2	63
16A-46	9320	1050	1.9	80
17D-18	9325	1050	1.4	75
17D-20	9325	980	1.7	63
17D-19	9325	950	1.3	63
17D-16	9325	830	1.4	55
17D-12	9325	1170	1.8	71
16A-3	9325	810	2.0	37
16A-40	9320	1000	2.0	80
26B-4	9245	1115	2.0	71
16 -13	9300	1115	2.2	180
27 -9	9325	780	1.9	100
27 -5	9325	770	1.8	70
27 -2	9350	985	2.4	130

NOTE: All high power test results were taken with:

- P_{IN} = 20 kW
- Pulse Width = 0.25 μs
- Duty Cycle = 0.001

TABLE I BULK LIMITER TEST RESULTS

BULK LIMITER	VSWR	INSERTION LOSS (dB)
16A-12	1.3	0.8
16A-2	1.45	0.7
16A-47	1.32	0.7
17D-13	1.32	0.7
16A-45	1.27	0.7
16A-1A	1.36	0.6
17A-42	1.34	0.7
16A-46	1.28	0.6
17D-18	1.31	0.6
17D-20	1.33	1.0
17D-19	1.38	0.9
17D-16	1.43	1.2
17D-12	1.60	0.8
17A-3	1.48	0.7
16A-40	1.29	0.8
26B-4	1.50	0.9
16A-13	1.33	0.7
27 -9	1.53	1.2
27 -5	1.53	1.1
27 -2	1.38	0.9

NOTE: Data shown represents maximum values taken in a swept frequency measurement. The required measurement for VSWR is 1.7, maximum; for insertion loss it is 1.3 dB, maximum.

TABLE II BULK -- CLEAN-UP LIMITER PACKAGE LOW POWER TEST RESULTS

IV. CONCLUSION

Confirmatory Samples, consisting of twenty (20) X-band bulk limiters and multi-stage clean-up diode limiters have been assembled. Bulk limiters were fabricated from high resistivity silicon with ρ = 8,000 - 15,000 ohm-cm, p-type, uncompensated $\langle 111 \rangle$ orientation from Wacker Chemical Company. These bulk limiters exhibit 3.0 dB bandwidth of 0.71 - 1.2 GHz and low insertion loss of 0.4 - 0.6 dB.

V. PROGRAM FOR THE NEXT QUARTER

During the next quarter, Confirmatory Samples will be submitted to Quality Control for environmental testing according to Specification SCS-486. The high power life test will be conducted on the bulk limiter assemblies.

VI. IDENTIFICATION OF PERSONNEL

During this quarter, the following technical personnel contributed to this program.

TITLE	MANHOURS
Project Manager	25
Processing Engineer	5
Limiter Engineer	5
Engineering Assistant (Fabrication)	15
Engineering Assistant (Test)	720
Assembly / Process	860

Electronic Command

Technical Requirements

SCS-486

28 March 1975

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts

MIL-STD-1311A Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

FSC 5961

REQUIREMENTS:

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-40B/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1 μsec pulses continuous	:	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss	:	0.7dB (max)
(c)	Low Level VSWR	:	1.4:1 (max)
(d)	Recovery Time	:	0.8μsec (max)
(e)	Flat Leakage	:	50 mw (max), for 30 kw, .001 duty cycle, 1μsec pulse
(f)	Spike Leakage	:	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias	:	none

3.4 Absolute Ratings

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

4.1.2 Test equipment c inspection facilities. - Test equi, ent and inspection facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance Inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection, tightened inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance number of zero (0). For purposes of inspection, the lot size shall be one (1) month's production.

4.4.3 Quality conformance inspection - Part 3 (QCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures shall be permitted.

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

4.6 —— Test Conditions

Parameter Unit	T_A °C	Fo GHZ	Po Watts	τ μsec	P_{RR} Pulses/sec	Du	Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 - 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μ sec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Table I

Quality Conformance Inspection - Part I (QCI-1)

Table II

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	No.
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0 0 0	db mw μ sec	10

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_i		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	γ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC111-3)

NOTES:

The maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4452 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

A swept frequency may be used.

Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

The firming power shall be defined as a db increase of limiter insertion loss compared to the "cold" insertion loss.

Quality conformance test to be made using bulk semiconductor stage only.

For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5μsec from the cessation of 1μsec input pulse.

Measurement of parameters cited will follow the procedures outlined in QCI -1.

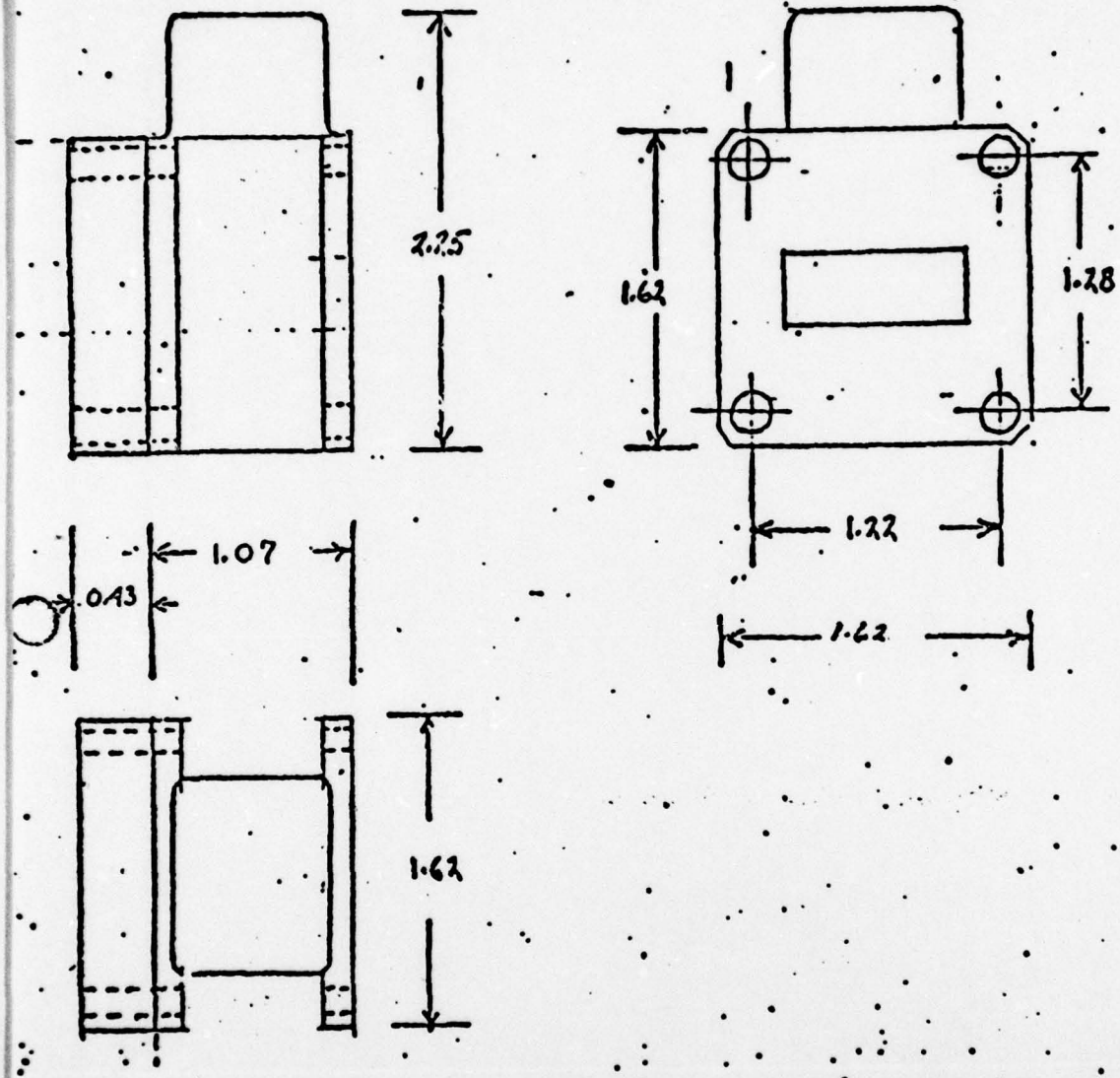
The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage (P_s), will be periodically monitored. Life test will be interrupted each 720 ± 20 hours interuals to permit testing of end of life test end points.

5. PREPARATION FOR DELIVERY

5.1 Packaging, Packing and Marking. - Packaging, packing and package arking shall be specified in the contract.

IGURE 1

LINE DRAWING



Notes:

a) all dimensions in inches

b) all tolerances ± 0.01 unless otherwise specified

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